WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a first semiconductor layer formed in a first region of a semiconductor substrate;

a second semiconductor layer formed in a second region of the semiconductor substrate with an insulation film interposed between the semiconductor substrate and the second semiconductor layer; and

a third semiconductor layer formed in a third region of the semiconductor substrate with the insulation film and a part of the second semiconductor layer extending in the third region and interposed between the semiconductor substrate and the third semiconductor layer, a top surface of the third semiconductor layer being higher than a top surface of the second semiconductor layer in the second region.

2. The semiconductor device according to claim 1, wherein the top surface of the second semiconductor layer in the second region is substantially flush with a top surface of the second semiconductor layer in the third region.

3. The semiconductor device according to claim 1, further comprising:

a MOS transistor provided on the third semiconductor layer; and

a fourth semiconductor layer formed on the second semiconductor layer in the third region so as to be

isolated from the third semiconductor layer, the fourth semiconductor layer being electrically connected to the third semiconductor layer via the second semiconductor layer.

4. The semiconductor device according to claim 3, further comprising a MOS transistor provided on the second semiconductor layer in the second region and having source and drain regions which reach the insulation film, and

wherein bottoms of source and drain regions of the MOS transistor provided on the third semiconductor layer exist within one of the second and third semiconductor layers, and a given potential is applied from the fourth semiconductor layer to the third semiconductor layer through the second semiconductor layer immediately under the source and drain regions.

5. The semiconductor device according to claim 4, further comprising an element isolation region which is formed in the third semiconductor layer and whose bottom exists in one of the second and third semiconductor layers,

wherein the element isolation region surrounds the MOS transistor provided on the third semiconductor layer, and a given potential is applied from the fourth semiconductor layer to the third semiconductor layer through the second semiconductor layer immediately under the source and drain regions and the element

isolation region.

6. The semiconductor device according to claim 1, further comprising:

a MOS transistor provided on the second semiconductor layer in the second region and having source and drain regions which reach the insulation film; and

a MOS transistor provided on the third semiconductor layer and having source and drain regions which reach the insulation film.

7. The semiconductor device according to claim 1, further comprising:

a DRAM cell provided at least on the first semiconductor layer; and

a logic circuit provided on the second and third semiconductor layers, the logic circuit controlling the DRAM cell.

8. The semiconductor device according to claim 1, wherein the third semiconductor layer has a thickness which is substantially equal to that of the first semiconductor layer.

9. The semiconductor device according to claim 1, wherein the third semiconductor layer has a thickness which is smaller than that of the first semiconductor layer.

10. The semiconductor device according to claim 4, wherein the MOS transistor provided on the second semiconductor layer is a partially-depleted type.

11. The semiconductor device according to claim 6, wherein the MOS transistors provided on the second and third semiconductor layers are a fully-depleted type and a partially-depleted type, respectively.

12. A method for fabricating a semiconductor device comprising:

forming a first insulation film, a first semiconductor layer, and a second insulation film in sequence in first to third regions of a semiconductor substrate;

removing the first insulation film, the first semiconductor layer, and the second insulation film in the first region and the second insulation film in the third region;

selectively forming a second semiconductor layer in the first region of the semiconductor substrate and on the first semiconductor layer in the third region; and

removing the second insulation film.

13. The method according to claim 12, further comprising measuring a thickness of the second semiconductor layer in the third region after the second semiconductor layer is formed.

14. The method according to claim 12, further comprising polishing the second semiconductor layer in the third region using the second insulation film in the second region as a stopper after the second

semiconductor layer is formed.

15. The method according to claim 12, further comprising forming semiconductor elements on the first semiconductor layer and the second semiconductor layer after the second insulation film is removed.

16. The method according to claim 15, wherein at least one of the semiconductor elements formed on the first semiconductor layer is a fully-depleted type MOS transistor, and at least one of the semiconductor elements formed on the second semiconductor layer in the third region is a partially-depleted type MOS transistor.

17. The method according to claim 15, wherein any one of the semiconductor elements formed on the second semiconductor layer in the first region is a DRAM cell.

18. The method according to claim 13, wherein the measuring comprises:

measuring a thickness of the first semiconductor layer in the second region by optical means;

measuring a thickness of a layered film of the second semiconductor layer and the first semiconductor layer in the third region by optical means; and

subtracting the thickness of the first semiconductor layer from the thickness of the layered film to calculate a thickness of the second semiconductor layer.

19. The method according to claim 13, wherein the

measuring comprises optimizing a deposition condition of a next deposition process in a deposition apparatus which forms the second semiconductor layer, based on a measurement result of the thickness of the second semiconductor layer.

20. The method according to claim 12, wherein the second insulation film functions as a mask against deposition of the second semiconductor layer, and is formed of materials which prevent the second semiconductor layer from being deposited on the second insulation film.

21. The method according to claim 20, wherein the second insulation film is formed of one of a silicon oxide film and a silicon nitride film.